Algorithms and Architectures for the Multirate Additive Synthesis of Musical Tones

by

Desmond Keith Phillips

A doctoral thesis submitted in partial fulfilment of the requirements for the award of

Doctor of Philosophy

School of Engineering, Durham University, UK

December 1996

Abstract

In classical Additive Synthesis (AS), the output signal is the sum of a large number of independently controllable sinusoidal partials. The advantages of AS for music synthesis are well known as is the high computational cost. This thesis is concerned with the computational optimisation of AS by multirate DSP techniques. In note-based music synthesis, the expected bounds of the frequency trajectory of each partial in a finite lifecycle tone determine critical time-invariant partial-specific sample rates which are lower than the conventional rate (in excess of 40kHz) resulting in computational savings.

Scheduling and interpolation (to suppress quantisation noise) for many sample rates is required, leading to the concept of Multirate Additive Synthesis (MAS) where these overheads are minimised by synthesis filterbanks which quantise the set of available sample rates. Alternative AS optimisations are also appraised. It is shown that a hierarchical interpretation of the QMF filterbank preserves AS generality and permits efficient context-specific adaptation of computation to required note dynamics. Practical QMF implementation and the modifications necessary for MAS are discussed. QMF transition widths can be logically excluded from the MAS paradigm, at a cost. Therefore a novel filterbank is evaluated where transition widths are physically excluded.

Benchmarking of a hypothetical orchestral synthesis application provides a tentative quantitative analysis of the performance improvement of MAS over AS. The mapping of MAS into VLSI is opened by a review of sine computation techniques. Then the functional specification and high-level design of a conceptual MAS Coprocessor (MASC) is developed which functions with high autonomy in a loosely-coupled master-slave configuration with a Host CPU which executes filterbanks in software. Standard hardware optimisation techniques are used, such as pipelining, based upon the principle of an application-specific memory hierarchy which maximises MASC throughput.

Acknowledgements

In memory of Leslie Phillips (1924-1996) to whom I owe my delight for discovery. Thankfulness is also due to my mother, and the many friends made during these epic years as an academic gypsy, for their steadfast loyalty. My supervisors, Prof. Alan Purvis and Dr. Simon Johnson, and fellow colleagues in Durham Music Technology are also to be mentioned for their encouragement, expertise and positive criticism.

Blessed Cecilia, appear in visions
To all musicians, appear and inspire
Translated Daughter, come down and startle
Composing mortals with immortal fire.

- W. H. Auden, “Song for St. Cecilia’s Day”, 1940

Contents

1. Introduction *1*

1.1 A Tutorial on 'Classical' Additive Synthesis **1**

1.1.1 Definition and Properties 1

1.1.2 Disadvantages 2

1.1.3 Piecewise Linear Envelope (PWL) Modelling of Envelopes 3

1.2 On the Specification of an Ideal Oscillator Bank **4**

1.2.1 Performance Criteria 4

1.2.2 Design Constraints 5

1.3 Conventional Solutions to AS Computation **5**

1.3.1 The Analogue Background to Digital AS 5

1.3.2 The Traditional Oscillator Bank 6

1.3.3 Impact of New Technology 9

1.4 Thesis Research Direction **10**

1.4.1 Optimisation of Sample Rate in Note-Based AS 10

1.4.2 Determination of Optimal Sample Rates 12

1.4.3 A Proposal for Multirate Additive Synthesis 15

1.4.4 Thesis Structure 16

1.4.5 Publications Arising from Thesis Research 18

2. Additive Synthesis: Context and Development *19*

2.1 Overview **19**

2.2 Alternative Synthesis Techniques **19**

2.2.1 Processed Recording 19

2.2.2 Physical Modelling 21

2.2.3 Abstract Algorithm 23

2.3 Developments in Spectral Modelling **24**

2.4 IFFT Simulation of the TOB **31**

2.4.1 Overlap-Add Synthesis 32

2.4.2 Supporting Frequency Envelopes 33

2.4.3 Noise Synthesis 34

2.4.4 Performance Evaluation 35

2.5 Review 36

3. Multirate Additive Synthesis *37*

3.1 Overview 37

3.1.1 Interpolation and Decimation in Multirate DSP 38

3.1.2 Efficient Interpolator Design 40

3.1.3 A General Model for MAS using Subband Decomposition 41

3.1.4 On Oscillator Q 43

3.1.5 Non-Overlapping Subband Decompositions 44

3.1.6 Overlapping Subbands 45

3.1.7 Towards an Objective Efficiency Comparison between AS and MAS 46

3.2 Proposal for a MAS Algorithm using QMF Filterbanks 48

3.2.1 QMF Filterbanks 48

3.2.2 QMF Subband Hierarchy 49

3.2.3 Allocation of {fmin(x), *fmax(x)}* in a Subband Hierarchy 51

3.3 A Comparison of AS via IFFT and Multirate Techniques 53

4. Practical QMF Filterbank Design *55*

4.1 Overview 55

4.2 FIR QMF Filterbank Design 56

4.2.1 Optimal Structure for a FIR QMF Stage 56

4.2.2 FIR Frequency Response Optimisation 57

4.3 MAS Normalisation Techniques for QMF FIR Filterbanks 59

4.3.1 Latency Normalisation 59

4.3.2 Frequency Normalisation 60

4.3.3 Phase Normalisation 61

4.4 IIR QMF Design 63

4.4.1 Normalisation with Non-linear Phase 65

4.5 Comparing PM-FIR and PA-IIR Performance for MAS 67

4.6 On Non-infinitesimal Δ_f in a Subband Hierarchy 68

4.7 Review 69

5. On the Exclusion of Filterbank Deadbands *71*

5.1 Overview 71

5.2 Logical Exclusion in QMF Filterbanks 71

5.2.1 A Formal Allocation Algorithm 71

5.2.2 Allocation Maps for Logical Exclusion 72

5.2.3 The Implications of Allocation Maps for PM-FIR and PA-IIR Filterbanks 74

5.3 Physical Exclusion Filterbanks 74

5.3.1 Discrete-Time Complex Signals 74

5.3.2 PEF Filterbank Design 75

5.3.3 Determination of Oversampling Factor λ 78

5.3.4 Latency Normalisation 79

5.3.5 Frequency Normalisation 79

5.3.6 Phase Normalisation 79

5.3.7 Functionally Equivalent Parallel-Form PEF Filterbanks 81

5.3.8 Simulation 82

5.4 Review 83

5.5 PEF Simulation Results 84

6. On Predicting a Performance Benchmark *86*

6.1 Overview 86

6.2 Description of The SHARC Timbre Database 87

6.3 Allocation Simulation for Orchestral Synthesis 89

6.3.1 Overview of Experiment 89

6.3.2 Preprocessing of SHARC Data 90

6.3.3 Organisation of Score and Orchestration Data 92

6.3.4 ALLOCSIM.C Algorithm 93

6.3.5 Analysis of the Allocation Histograms 94

6.4 Benchmark Calculation 96

6.4.1 Quantifying MAS Overheads 96

6.4.2 Filterbanks: Quantity, Topology and Cost 97

6.4.3 Applying Allocation Simulation Data 100

6.4.4 Analysis of Benchmarking Results 101

6.5 Review 102

6.6 Benchmark Results 103

7. Digital Sine Oscillator Design *106*

7.1 Overview **106**

7.2 Recursive Oscillators **107**

7.2.1 The Biquad Oscillator 107

7.2.2 The Coupled Form Oscillator 108

7.2.3 The Modified Coupled form Oscillator 110

7.2.4 The Waveguide Oscillator 111

7.2.5 Review of Recursive Oscillator Designs 112

7.3 Phase-Accumulator Oscillators **113**

7.4 Efficient Sine Calculation **114**

7.4.1 Taylor's Series 114

7.4.2 Look-Up Tables 115

7.4.3 Linear Interpolated Look-Up Tables 116

7.4.4 Dither in Look-Up Tables 118

7.4.5 Review 118

7.5 CORDIC Vector Rotation Algorithm **118**

7.5.1 Definition 118

7.5.2 Application to Complex Oscillators 119

7.5.3 VLSI Implementation of CORDIC 121

7.5.4 Complex Oscillator Core with a CORDIC Pipeline 122

7.5.5 Determination of CORDIC S/N Performance from *M* and *N* 123

7.6 Conclusions **125**

8. Specifying MAS Coprocessor Functionality *126*

8.1 Overview **126**

8.2 On the Economics of an ASIC-based MAS Implementation **127**

8.3 Processes and Control Data in Real-Time MAS **128**

8.3.1 Logical Process Pipeline 128

8.3.2 Control Data Proliferation 130

8.4 Mapping Processes to Processors **131**

8.4.1 High-Level Multiprocessor Topologies 131

8.4.2 Interprocessor Communication via Shared Memory 132

8.5 Specifying MASC - SM Traffic 135
8.5.1 The Oscillator Descriptor 135
8.5.2 Interleaved Burst Processing 138
9. Towards A MASC Design ***142***
9.1 Overview 142
9.2 MASC Functional Requirements for MAS 142
9.2.1 Supporting Multiple Sample Rates for MAS by Frame Scheduling 142
9.2.2 Burst Accumulation of Subband Streams 144
9.3 Scheduling, Resource Allocation and Synchronisation 146
9.3.1 Data Structures and Algorithms for Scheduling and Resource Allocation 146
9.3.2 Frame-Level Process Synchronisation 147
9.4 Quantitative Aspects of MASC Implementation 151
9.4.1 On the Interdependency of MAS Latency and MOB Burst Length 151
9.4.2 Quantifying Expected MASC throughput 152
9.4.3 Quantifying the SM Bandwidth Requirement of Host / FBP IPC 154
9.5 Dataflow Aspects of MASC Design 156
9.5.1 Systems-Level MASC Architecture 156
9.5.2 Prefetch and Writeback Buffers 157
9.5.3 PWL Envelope ALU 157
9.5.4 Accumulation Structure 159
9.5.5 Header Word Processing in the Control Unit 160
9.6 Review 161
10. Conclusions and Further Work ***162***
Appendix A: SHARC Database Structure ***166***
Appendix B: Orchestration of Enigma Variations ***167***
References ***168***
Bibliography ***177***
Glossary of Terms ***179***
Abbreviations 179
Commonly Used Mathematical Symbols 181

Figures

Figure 1.1 PWL Approximation of a Trumpet Note 3
Figure 1.2 Traditional Oscillator Bank 7
Figure 1.3 The Role of an Oscillator Bank in Spectral Modelling 8
Figure 1.4 Frequency Envelopes for Grey's Trumpet 13
Figure 2.1 Overlap-Add IFFT Synthesis with Triangular Windows 32
Figure 3.1 Interpolation and Decimation of Sinusoids 38
Figure 3.2 A General Model of Multirate Additive Synthesis 42
Figure 3.3 Classic Subband Decompositions 44
Figure 3.4 Fully and Partially Overlapping Octave-spaced Series for K=5 46
Figure 3.5 E versus v(K) given n 47
Figure 3.6 Operation of QMF Synthesis Filterbank Stage 49
Figure 3.7 Example QMF Filterbank and Subband Hierarchy for K=3 50
Figure 3.8 Evolution of Subband Hierarchy Allocation Pattern with Increasing τ 52
Figure 3.9 υ *versus* τ 53
Figure 4.1 Unwindowed FIR Responses for $h0[m]$ *and* $h1[m]$ *for M=11, N=23* 56
Figure 4.2 Optimal Realisation of FIR QMF Synthesis Stage 57
Figure 4.3 FIR designs for H0(z) with Δ_f*=0.1,* $\delta_p=\delta_s$*=-80dB* 59
Figure 4.4 Trapezoidal Integration of Decimated Frequency Envelope 61
Figure 4.5 Phase Response of PA-IIR Filter 64
Figure 4.6 IIR Polyphase Allpass QMF Synthesis Stage 65
Figure 4.7 PA-IIR H0(z) Response 65
Figure 4.8 Required Passband Phase Response of P(z) 66
Figure 4.9 Deadbands in Spectral Hierarchy due to Non-infinitesimal Δ_f 68
Figure 5.1 Logical Exclusion Allocation Maps for Δ_f*=0.0,* Δ_f*=0.05 (K=3)* 73
Figure 5.2 Spectra of Discrete-Time Complex and Single-Phase Signals 75
Figure 5.3 Frequency Domain Operation of PEF Stage 76
Figure 5.4 PEF Stage Dataflow 77
Figure 5.5 PEF Filterbank Topology for Depth K=3 77
Figure 5.6 FIR M versus λ 78
Figure 5.7 Path Model from Level k in a PEF Filterbank 80
Figure 5.8 110Hz (A1) Sawtooth without Phase Normalisation 84
Figure 5.9 110Hz (A1) Sawtooth with Phase Normalistion 84
Figure 5.10 27.5Hz to 440Hz (A0 to A4) Chirped Sawtooth 85
Figure 6.1 Dataflow of Allocation Simulation 90

Figure 6.2 Subband Hierarchy and Filterbank Topology Used in Simulation ____ *97*
Figure 6.3 'C.A.E.' Allocation Histograms ____ *103*
Figure 6.4 'Nimrod' Allocation Histograms ____ *103*
Figure 6.5 E1 for 'C.A.E.' ____ *104*
Figure 6.6 E1 for 'Nimrod' ____ *104*
Figure 6.7 E2 for 'C.A.E.' ____ *105*
Figure 6.8 E2 for 'Nimrod' ____ *105*
Figure 7.1 The Biquad Oscillator ____ *108*
Figure 7.2 The Coupled form Oscillator ____ *109*
Figure 7.3 The Modified Coupled form Oscillator ____ *110*
Figure 7.4 The Second Order Digital Waveguide Oscillator ____ *112*
Figure 7.5 The Phase-Accumulator Oscillator ____ *113*
Figure 7.6 Max Error (dB) of nth order Taylor's Series approximation for sin(θ) ____ *115*
Figure 7.7 Pipeline Form of Interpolating LUT Oscillator ____ *117*
Figure 7.8 Dataflow for ith stage of CORDIC vector rotation ____ *121*
Figure 7.9 Schematic Diagram of CORDIC-based Complex Oscillator Core ____ *123*
Figure 7.10 CORDIC Oscillator Performance ____ *124*
Figure 8.1 Comparison of the Economics of Software and ASIC Implementations ____ *127*
Figure 8.2 Processes and Control Data Bandwidth in a MAS Synthesiser ____ *129*
Figure 8.3 Architectural Forms of Multiprocessor MAS Synthesiser ____ *131*
Figure 8.4 Oscillator Descriptor Organisation ____ *136*
Figure 8.5 Interleaved Burst Processing ____ *140*
Figure 8.6 Model of MAS Memory Hierachy ____ *141*
Figure 9.1 Extended Burst of $2N_{burst}$ for Subbands at Level k=K-1 ____ *143*
Figure 9.2 Accumulation Burst Timing ____ *145*
Figure 9.3 Minor / Major Runs in the OD Schedule ____ *147*
Figure 9.4 MASC Synchronisation for $n_{fb}=4$ ____ *148*
Figure 9.5 Schematic Diagram of MASC Architecture ____ *156*
Figure 9.6 Prefetch and Writeback Buffers ____ *157*
Figure 9.7 Dataflow for $A_i[n]$ and $F_i[n]$ Structures ____ *158*
Figure 9.8 Dataflow for $\Phi_i[n]$ Structure ____ *159*
Figure 9.9 Accumulation Structure Dataflow ____ *159*

Tables

Table 4-1 Relative Complexity of FIR and PA-IIR QMF Stages _____ *67*

*Table 5-1 Equivalent Filterbank Performance for K=3*_____ *81*

Table 6-1 Filterbank Cost v _____ *99*

Table 7-1 Summary of Recursive Oscillator Features _____ *113*

*Table 9-1 OD Header Word Bitfield Assignment*_____ *160*

I confirm that the thesis conforms with the prescribed word length for the degree for which I am submitting it for examination.

I confirm that no part of the material offered has previously been submitted by me for a degree in this or any other University. If material has been generated through joint work, my independent contribution has been clearly indicated. In all other cases material from the work of others has been acknowledged and quotations and paraphrases suitably indicated.

Signed: .....

Dated: .....